
Claims

1. A method for sampling an analog input signal and storing digital presentation said samples in a memory, said method comprising:

generating a sequence of clock pulses at a predetermined frequency F_{clk};
generating a pseudo-random integer A ranged from K to K+N where K and N are predetermined constants equal to one or greater than one, at every sampling pulse;
dividing said sequence of clock pulses by said integer A to select one last pulse from every series of A clock pulses;
forming a sequence of sampling pulses from said sequence of selected clock pulses by means of the following steps:
(a) generating a pseudo-random integer B ranged from zero to M, where M are predetermined constants equal to one or greater than one, in parallel with said integer A;

(b) delaying the selected clock pulse by value DxB, where D is equal to $1/F_{clk}(M+1)$; and
sampling an analog input signal at said delayed clock pulse, and converting the said sample value to a predetermined digital format; and
storing the current signal sample value in a memory.

2. The method of claim 1, wherein said method is adapted to sampling an analog input signal at the highest rate; and wherein said integer A is equal to one if said integer B is greater than its preceding value; otherwise it is equal to two.

3. A digitizer adapted to sample an analog input signal, store the digital values representing said signal sample values in a memory, and further process digitally said digital values; said digitizer comprising:
a clock producing a sequence of electrical pulses at predetermined frequency;
a random number generator adapted to generate a pseudo-random integer A ranged from K to K+N where K and N are predetermined constants equal to one or greater than one, the value of said integer A changing after each sampling pulse;
a divider adapted to count said clock pulses and produce one output pulse for series of A clock pulses;
means for forming a sequence of sampling pulses having:

(a) a pseudo-random number generator adapted to generate a pseudo-random integer B ranged from one

to M, said integer B changing after each sampling pulse;

(b) a digitally controllable pulse delay block adapted to delay said selected pulse by a value DxB, where D is a minimum delay increment equal to $1/F_0(M+1)$;

an analog-to-digital (``A/D'') converter adapted to sample said analog input signal and produce a digital output value that is a digital presentation of said analog input signal at each of said divided and delayed clock pulses;

a memory adapted to receive said digital output value from said A/D converter, and to store said digital output values after its receiving.

4. The apparatus of claim 3, wherein said random number generators are a memory adapted to produce cyclically a series of said integers A and B when triggered by a control signal, the series of said digital values A and B is before pre-calculated and stored in said memory.